IN THE DRAWINGS:

Please amend figure 3 with enclosed new FIG 3 marked "replacement sheet".

REMARKS

Reconsideration of the above-identified application in view of the amendments to the claims and the following remarks is respectfully requested.

Claims 1-12 are rejected. Claim1, 3-5, 8-9, and 11-12 have been amended and claim 10 has been canceled. Claims 1 and 9 are independent claims. Claims 1-12 are pending.

Claims 1 and 9 have been amended to incorporate a limitation disclosed in dependent claim 3 and 10. Claim 10 has been canceled. Dependent claims 11-12 have been amended to reflect proper dependency.

The drawings stand objected to under 37 CFR § 1.83(a) because of missing structure described in the specification but not provided for in the drawings. According to the Office Action, FIG. 2, reference character 27 fails to show the reset input signal shown in FIG. 3 in FIG. 2. In response, applicant herein submits a replacement figure 3 to overcome the Examiner's objection.

Claim 5 and 8 stands objected to for informalities. In response, applicants have amended dependent claim 5 to reflect proper dependency to dependent claim 4. In addition, dependent claim 8 has been amended to define acronyms HD and SD.

Therefore, applicants request withdrawal of the objections to dependent claims 5 and 8.

Claims 3-5 stand rejected under 35 USC § 112, second paragraph because claims 3-5 are vague and indefinite. In response, applicants have corrected all three dependent claims to provide proper antecedent basis for the limitation 'a' sync byte, 'a' Ox47 byte, and, 'a' detected Ox47 byte.

Therefore, applicants request withdrawal of the rejections to dependent claims 3-5.

Claim 1 stands rejected under 35 USC § 102(a) as being anticipated by Applicant's Admitted Prior Art (US 2004/0234019)(hereinafter "AAPA").

Claim 1, as amended, recites an asynchronous transport stream receiver of a digital broadcasting receiving system comprising, *inter alia*, a controller for reading and outputting the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator, **the controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator**.

Accordingly, the AAPA fails to anticipate the present invention as it fails to show for example, a **controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator,** as recited in the amended base claim.

Therefore, applicants respectfully request withdrawal of this ground of rejection.

Claims 1, 2 and 7 stand rejected under 35 USC § 103(a) as being unpatentable over Molloy (US 5,337,334) in view of Wei (US 2002/0154640). In addition, claim 9 stands rejected under 35 USC § 103(a) as being unpatentable over Venkata et al (US 2003/0052709) in view of Hui et al (US 6,868,091).

Claim 1, as amended, recites an asynchronous transport stream receiver of a digital broadcasting receiving system comprising, *inter alia*, a controller for reading and outputting the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator, **the controller including a PLL (Phase Locked Loop) or DLL**

(Dynamic Linking Library) for demultiplying the clock signals of the oscillator. Claim 9, as amended recites a similar method which provides demultiplied clock signals of the oscillator by a **predetermined number of times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals**. The terms "predetermined number of times" is supported in the specification for example on page 9, line 3 and page 10, line 18.

In contrast, Molloy discloses a synchronous digital signal to asynchronous digital signal desynchronizer where a digital phase locked loop, *inter alia* is provided to improve **jitter performance**. In the Office Action, reference character 106, found in Molloy's FIG.1 is erroneously identified as the PLL recited in dependent claim 3. Molloy, as read by applicant, discloses that phase detector 109 and sequential filter 110 and DCO 11 form a *digital phase locked loop*. As such, Molloy's PLL operates " . . . in response to the adjusted reference signal supplied from controllable divider 107 and adjusted phase control signal supplied from controllable divider 108 in overhead gap distribution circuit 106 to **generate the desired smooth read clock signal** . ..." (Col. 5, line 11-26) (Emphasis added).

The present invention on the other hand, operates to enhance the performance of the MPEG-2 data. As disclosed in the specification, "[i]n order to allow "MPEG-2 data to be outputted at the bit rate of up to 72 Mbps" . . . "the PLL 28 may be utilized at the FPGA 27" (as opposed to a DLL), for example;

> The clock signals of the 27 MHz oscillator 14 are inputted into the PLL 28 of the FPGA 27, and then when the clock signals are divided three times, the clock signals of 9 MHz can be obtained. When these 9 MHz clock signals are used as read clock signals, the FPGA 27 is then capable of reading and processing the MPEG-2 data of up to maximum 72 Mbps from the FIFO section 26. Further, the FPGA 27 matches the read MPEG-2 data with the clock signals divided at the

> PLL 28, and then transmits the matched results to the set-top box (not shown). Meanwhile, when the clock signals of the 27 MHz oscillator are divided 10/27 times, clock signals of 10 MHz can be obtained. Additionally, the MPEG-2 data can be outputted at the bit rate of 80 Mbps, matching the upper bound of the MPEG-2 data of the MP-HL.

(Page 8, line 21 to page 9, line 8).

In other words, Molloy fails to suggest or teach a, **controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator** as recited in amended base claim 1. Moreover, Molloy fails to suggest or teach a method of providing demutlplied clock signals of the oscillator by a **predetermined times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals** as recited in amended base claim 9.

Venkata, also fails to disclose a **PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator** or a method of providing demultiplied clock signals of the oscillator by a **predetermined times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals** as recited in amended claim 9. According to Venkatathe, the PLL circuitry is provided for use in the clock data recovery circuitry to support both 8B10B and POS-5 communication (page 2, paragraph [0010]. In other words, Venkatathe fails to suggest or teach a **controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator** as recited in amended base claim 1. Moreover, Venkatathe fails to suggest or teach a method of providing demutlplied clock signals of the oscillator by a **predetermined times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals** as recited in amended base claim 9.

The other references Wei and Hui, cited in the Office Action in support of the obviousness rejections are all silent on the use of a PLL. Therefore, they both fail to suggest or teach a **controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator** as recited in amended base claim 1. Moreover, Venkatathe fails to suggest or teach a method of providing demutlplied clock signals of the oscillator by a **predetermined times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals** as recited in amended base claim 9.

Therefore, applicants respectfully request withdrawal of the rejections of base claim 1 and 9 as none of the references suggest or teach a **controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator** as recited in amended base claim 1. Moreover, Venkatathe fails to suggest or teach a method of providing demutlplied clock signals of the oscillator by a **predetermined times** and **reading the MPEG data from the FIFO section in synchronization with the demultiplied clock signals** as recited in amended base claim 9.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of the patentability of each on its own merits is respectfully requested.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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